Overview

- Goals
- Program
- Summary

Summit Goals

- Bringing together European HPC Centers, EuroHPC, EC, and Industry

- Start the conversation about EU HPC Digital Sovereignty

- Understand where we are today with 4 use cases
    - Automotive, Life Science, Engineering & Weather/Climate

- Discuss what we need for the future with these 4 use cases

- General discussion about the future of EU HPC

- Start to define the future roadmap

- Rinse and Repeat

    https://www.bsc.es/news/events/barcelona-build-vs-buy-hpc-summit-3b4hpc

Thursday Morning Agenda

Time	Title	Speaker(s)
9:00 to 9:30	Intro and Goals - BSC Intro	Mateo Valero (BSC) John Davis (BSC)
9:30 to 10:00	Intro EURO HPC **"Towards a federated European HPC ecosystem"**	Daniel Opalka - EURO HPC Joint Undertaking (JU)
10:00 to 11:00	Keynote HPC HW/ SW Stack **"Fugaku Co-Designing from Genesis to Productive Present"**	Satoshi Matsuoka (RIKEN)
11:00 to 11:30	Break (30 mins)	LOCATION: Vertex Garden
11:30 to 12:30	Life Science SW/HW Stack **"Computational challenges in the future of molecular biology and Personalized Medicine"**	Arnau Montagud Aquino and Jose Carbonell (BSC)
12:30 to 13:30	Engr/IT/Industry SW/HW Stack **"Engineering Applications: CoE RAISE and Beyond"**	Thomas Lippert (Jülich Supercomputing Centre)
13:30 to 14:15	Lunch	LOCATION: BSC Foyer Capella Marenostrum 4
14:15 to 15:00	MN 5 tour	LOCATION: BSC HQ

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

Thursday Afternoon Agenda

Time	Title	Speaker(s)
15:00 to 16:00	Automotive SW/HW Stack **"Automotive/Engineering requirements on Hardware and Software - Today and Future"**	Bastian Koller and Andreas Wierse (HLRS)
16:00 to 17:00	Weather SW/HW Stack **ECMWF Part 1: operational models: Simulations in a data-rich environment (Thomas Geenen)** **ECMWF Part 2: Predicting trends to support Weather and Climate forecasts (Christine Kitchen)**	Christine Kitchen and Thomas Geenen (ECMWF)
17:00 to 17:15	Break	LOCATION: Vertex Garden
17:15 to 18:15	Industry Panel	Jean Marc Denis (Sipearl), Emmanuel Le Roux (ATOS) , Utz-Uwe Haus (HPE), Phil Thierry (Intel) , Gabriele Paciucci (Nvidia)
18:15 to 19:00	Shuttle pick up at Vertex - Travel to MNAC Museum	
19:00 to 20:00	MNAC Museum Tour/ Free Time	LOCATION: MNAC Museum Tour
20:00 to 22:00	Dinner @ Oleum MNAC Museu Nacional Art de Catalunya	LOCATION: Oleum MNAC Museu Nacional Art de Catalunya
22:30-	Shuttle pick up @MNAC - Travel to BSC HQ + Hotel Abba Garden	

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

Thursday Summary

- Update from the JU:
  - 32 participants (Serbia is a new member)
  - Exascale site (JSC) + 4 mid-range sites selected
  - Quantum in HPC
  - Updating the procurement strategy

- Retrospective on Fugaku
  - 10 year development cycle
  - Focused on Real App performance improvements
  - There is a dark-side to co-design: overfitting causes performance cliffs
  - RAS is critical with 160K nodes
  - Based on slight modifications to Fugaku technology, could do up to 3 ExaFLOPs in 20 MW
  - Next machine around 2029

Barcelona Supercomputing Center
Centro Nacional de Supercomputación
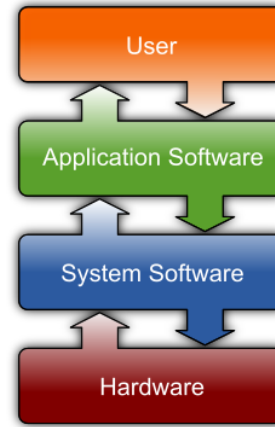
Setting the stage with 4 Use Cases

- 4 HPC use cases: Automotive, Engineering, Life Science and Weather
  - Research ⟷ Production SLAs and expectations
  - Still room for significant micro and macro scaling in the applications
    - Micro: Cloud features in weather and genomic interactions in cells
    - Macro: "digital twin" of the earth or human body
  - Moving Beyond BigData → Datasets continue to grow
  - Positive CoE collaborations
  - Bridging the TRL **CHASM** between 5-7
  - Solutions
    - Software
    - Silicon
    - Systems
    - Skills
  - New ways of procuring systems, multiple phase instead of every 5 years?

Barcelona
Supercomputing
Center
Centro Nacional de Supercomputación

The View from the IT Industry

- How do we define European added value?
  - Designed in Europe?
  - Made in Europe?
  - Head count in Europe?
- EU Digital Sovereignty has two (related) components
  - Freedom (from embargo)
  - Sustainable development in the EU
- In other regions, HPC is a strategic asset, why not in Europe?
- Research and Industry
  - Research collaborations
  - Co-design
  - Co-development
- No more Top500 as the main system spec.
- What about the cloud?

Friday Morning Agenda

Time	Title	Speakers
9:00 to 9:30	Introduction/Recap	John Davis (BSC)
9:30 to 10:00	EPI GPP: SiPearl **"How a European Research and Innovation project has become a successful industrial story"**	Jean-Marc Denis (Sipearl)
10:00 to 10:30	EPI EPAC: **RISC-V "accelerator" in EPI**	Jesús Labarta (BSC)
10:30 to 11:00	Quantum Computing in EU **"Towards EuroQCS – the European Quantum Computer and Simulation infrastructure"**	Kristel Michielsen (Juelich)
11:00 to 11:30	Break	LOCATION: Vertex Garden
11:30 to 13:00	HPC Center HW Panel	Alfonso Valencia (BSC), Bastian Koller (HLRS) , Chris Kitchen (ECMWF), Estela Suarez (Jülich)
13:00 to 14:30	Lunch	LOCATION: Vertex Garden

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

Friday Afternoon Agenda

Time	Title	Speakers
14:30 to 16:00	Panel on Future HPC Systems (HW & SW)	Satoshi Matsuoka (RIKEN), Mateo Valero (BSC), Thomas Lippert (Jülich), Jean-Philippe Nominé (CEA)
16:00 to 16:30	Break	LOCATION: Vertex Garden
16:30 to 18:00	Discussion, Wrap Up, next steps...	BSC leads discussion
18:00 to 20:00	Dinner at BSC	LOCATION: BSC Foyer Capella Marenostrum 4
20:30	Shuttle pick up @BSC - Travel to Hotel Abba Garden	

Barcelona
Supercomputing
Center
Centro Nacional de Supercomputación

Friday Presentations

- SiPearl
  - Company rapidly growing
  - Developing a big ecosystem with many partners
  - Build (⚙) vs Buy ($)Value Chain
    - IP (⚙/$) → Design (⚙) → Manufacturing (⚙/$) → System Integration (⚙/$) → HPC Centers
  - 2 Big challenges
    - **Skilled workforce**
    - **European funding**

- EPAC: RISC-V Accelerators (Vision Important)
  - STX: AI & Stencil
  - RVV: Self-hosted, general purpose vector SMP
  - VRP Extended precision arithmetic
  - RVV @ FPGA & Ecosystem
  - EPAC V1.5 tapeout in August 2022
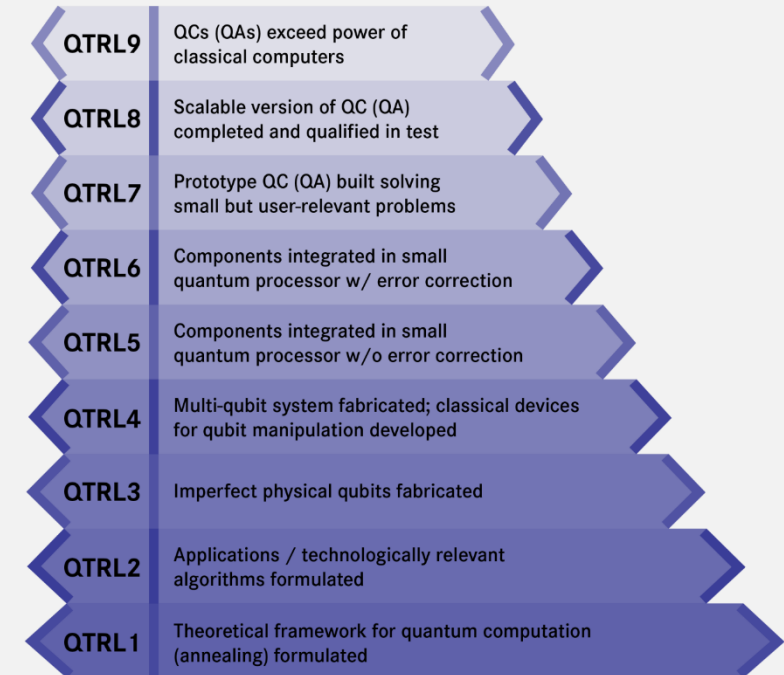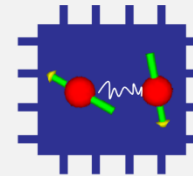

Vector register file (8 lanes)
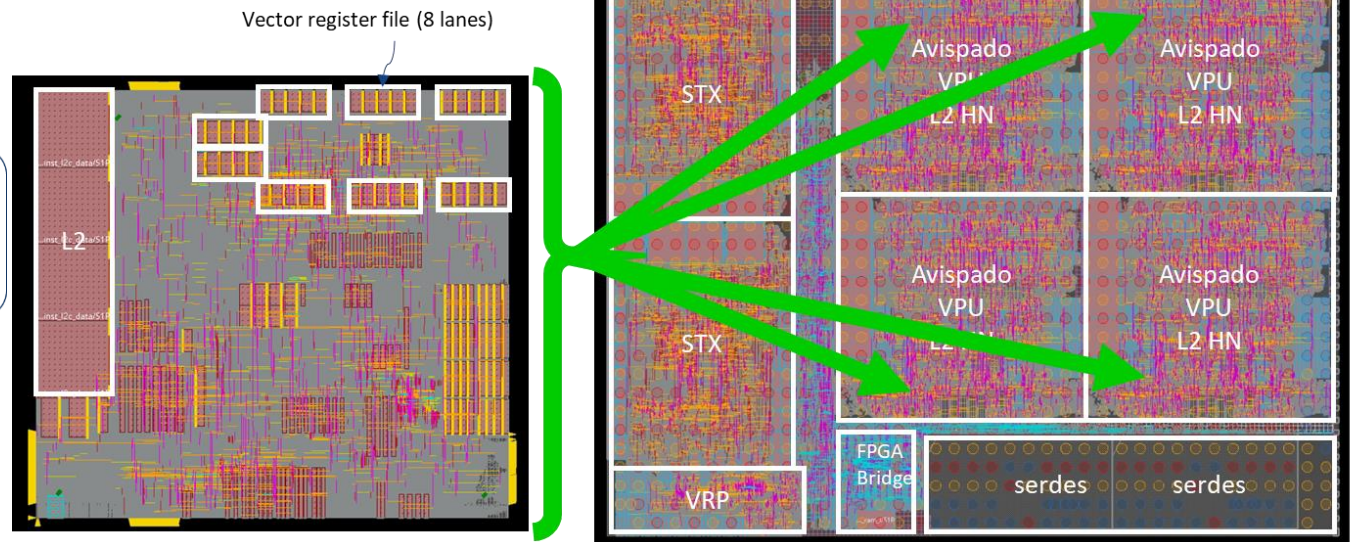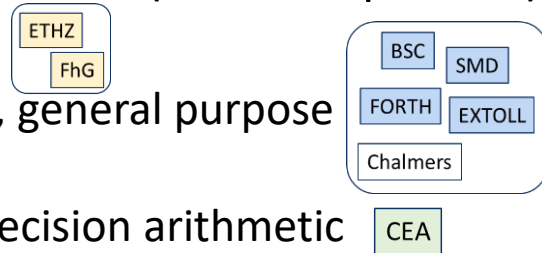
Friday Presentations Cont...

- Quantum
  - No clear killer app for Quantum
  - Maturity of Quantum Computers (QC)
    - Quantum Technology Readiness Levels: QTRL1 to QTRL9
  - Huge challenge and opportunity
    - Applications and use case for quantum simulators, computers and annealers
  - Classic HPC Systems + Quantum computers and Simulators
  - High Performance Computer and Quantum Simulator hybrid
    - Dec 1, 2022 – Nov 30, 2025
    - Coordinator: Forschungszentrum Jülich GmbH
    - 15 partners + 3 linked 3rd parties from 6 countries
    - Prepare Europe for the use and federal operation of quantum computers (QC) and simulators (QS)
    - Develop, deploy and coordinate a European federated infrastructure integrating a QS of 100+ interacting quantum units in the HPC systems of the supercomputer centres FZJ/JSC and GENCI/CEA
    - Provide cloud access for European users, on a non-commercial basis
  - EUROHPC-2022-CEI-QC-01, recent call (June 2022) to host QCs

QTRL

Quantum Technology Readiness Levels describing the maturity of Quantum Computing Technology

QTRL9	QCs (QAs) exceed power of classical computers
QTRL8	Scalable version of QC (QA) completed and qualified in test
QTRL7	Prototype QC (QA) built solving small but user-relevant problems
QTRL6	Components integrated in small quantum processor w/ error correction
QTRL5	Components integrated in small quantum processor w/o error correction
QTRL4	Multi-qubit system fabricated; classical devices for qubit manipulation developed
QTRL3	Imperfect physical qubits fabricated
QTRL2	Applications / technologically relevant algorithms formulated
QTRL1	Theoretical framework for quantum computation (annealing) formulated

Barcelona Supercomputing Center
Centro Nacional de Supercomputación
BSC

Friday Panels

- HPC Center (HW) based on the 4 Use Cases
  - HPC improvements
    - Need to address the imbalance between compute and memory bandwidth.
    - It would be great to have performance portability.
    - Large-scale cluster management is a challenge from multiple dimensions: RAS, performance, energy, dynamic scaling, fault tolerance, working rolling updates…
    - Continuous integration with a software focus can be applied to the system, share best practices across centers.
  - Magic wand to improve the HPC Centers
    - Higher efficiency and better system management.
    - More partitions for development, more connectivity to other systems, better mapping of codes to accelerators, more performance for NLP and other problems.
    - Federation and the use of the cloud.

Friday Panels

- Future HCP Systems?
  - Vector architectures with support for sparse workloads (like graphs). Dynamic and malleable architectures.
  - Disaggregated systems that combine accelerators for DLP and super fast single thread performance to attack all parts of Amdahl's law.
  - Digital twins are the next killer app for HPC, however, need to dramatically reduce the cost of accelerators.
  - Build higher efficiency systems that are heterogeneous with islands at the micro and macro level. Can't forget about storage and networking.
  - Must support more complex workflows.
  - Need to address the cost structure in HPC. For weak scaling machines, too expensive per node (~$20K)
    - Fugaku node has the same performance as a Playstation 5, but not the same cost.
  - How do we move away from Linpack as a major system benchmark?
    - Only use real production codes as benchmarks
    - Base machine selection on peak performance numbers, assuming mature codes that can get close to peak.
  - Other major system components to consider beyond compute: Storage and Networking
  - Prediction: In 10 years, we will see RISC-V based HPC systems

Wrap-Up

- BSC proposal to change R&I and system procurement
  - Need infrastructure to support new model
    - Special Interest Group for HPC in RISC-V International
    - Laboratory for Open Computer Architecture and systems LOCA @ BSC
    - New linked programs: Flagship, CoE, FPA(s), and Procurement(s)
  - Link them together with money to build components and support the ecosystem. This should help cross the TRRL 5-7 Chasm.
  - Follow the Fugaku and ECP models
    - (BIG) Money for SW and HW development and system acquisition
      - > 1B€ for SW, > 1B€ for Accelerator HW, , > 1B€ for CPU HW, + machines
    - Accelerator or CPU development takes 3 years to get to silicon, once you have BIG money to pay for it.
  - For example, with MN6
    - Flagship program: Little research and large Development budget towards system
    - Connect the flagship to HPC system procurement, participants in flagship provide the final machine
    - Add Center of Excellence to drive innovation
    - Research $\rightarrow$ Prototype $\rightarrow$ Pilot $\rightarrow$ Emerging Technology $\rightarrow$ Production

Thank you all for coming!!

john.davis@bsc.es