Call for papers

15th International Workshop on Worst-Case Execution Time Analysis (WCET 2015)

July 7th, 2015. Lund, Sweden

http://www.bsc.es/caos/wcet2015

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The 15th International Workshop on Worst-Case Execution time Analysis (WCET 2015) is a satellite workshop of the 27th Euromicro Conference on Real-Time Systems (ECRTS 2015), the premier European venue for presenting research into the broad area of real-time and embedded systems. WCET 2015 is sponsored by TACLe (www.tacle.eu) European COST-Action, and the FP7 Projects PROXIMA (www.proxima-project.eu) and P-SOCRATES (www.p-socrates.eu). WCET 2015 is supported by the HiPEAC Network of Excellence (www.hipeac.net).

SCOPE

WCET workshop is the reference forum for academics, practitioners and industrials in any aspect related to the timing analysis of computer systems. While in the past timing analysis has been a topic mainly for real-time systems, recently it has becoming crucial in other domains dealing with timing guarantees. This includes among other mobile computing and high-performance computing. This edition of the WCET workshop, besides papers targeting traditional WCET analysis, encourages submissions focused on less rigorous and mature timing analysis techniques on complex multicore and manycore heterogeneous, usually COTS, architectures. For such complex architectures Execution Time Bound (ETB) estimates are derived rather than WCET estimates in the strict sense. ETB estimates are intrinsically less reliable than WCET estimates.

TOPICS

This workshop seeks original contributions on topics that include but are not limited to:

- WCET/ETB analysis for multi- and many-core systems
- WCET/ETB analysis for multi-threaded applications
- WCET/ETB analysis for COTS processors
- Case studies, and industrial experience of WCET/ETB analysis
- Timing Analysis and safety standards
- Different approaches to WCET/ETB computation
- Probabilistic timing analysis
- Tools for WCET/ETB analysis
- Timing-predictable operating systems and processor designs
- Compiler-based optimization of worst-case timing
- Low-level timing analysis, modelling and analysis of processor features
- Flow analysis for WCET, loop bounds, infeasible paths
- Integration of timing analysis and schedulability analysis
- Integration of timing analysis in development processes
- Methods and benchmarks for timing analysis evaluation

Innovative, controversial statements or that present new approaches are specially sought.

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IMPORTANT DATES

Paper submission: May 1, 2015
Notification of acceptance: May 22, 2015
Final paper submission: June 12, 2015
Workshop: July 7, 2015

GENERAL CHAIR

Francisco J. Cazorla Leader of the CAOS group at BSC and researcher at IIIA-CSIC.

SUBMISSION INSTRUCTIONS

Research papers should present original research results not published or submitted for publication in other forums. Authors of accepted papers agree to attend the workshop and to present their work during the workshop.

Papers submitted for the WCET workshop must be written in English, must not exceed 10 pages, should conform to the typesetting requirements specified on the workshop's website (http://www.bsc.es/caos/wcet2015), and must be submitted in PDF format using the WCET workshop paper submission website. Author names, affiliations and self-references should not be anonymized.

PROGRAM COMMITTEE

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