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Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

A Model for Building an Open HPC Ecosystem

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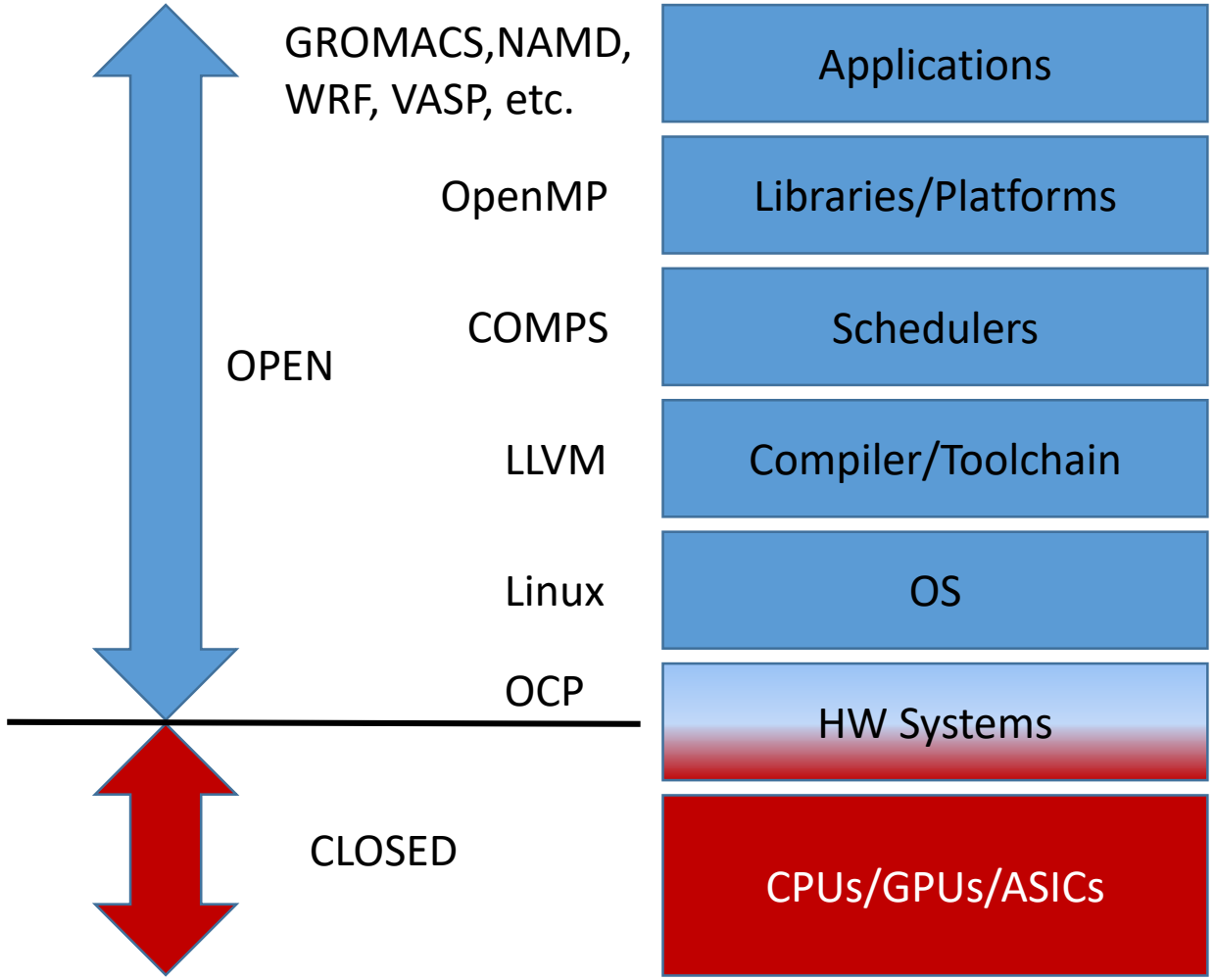
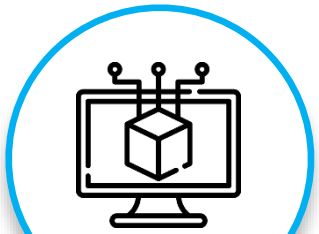
1/7/2022

HPC Today

- **Europe has led the way in defining a common open HPC software ecosystem**
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU and accelerators?**



Today´s technology trends



Massive penetration of Open Source Software

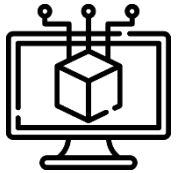
- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)

Moore´s Law + Power = **Specialization**

- More cost effective
- More performant
- Less Power

SOFTWARE/
HARDWARE
CO-DESIGN

Today´s technology trends



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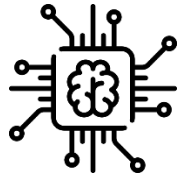


New Open Source Hardware Momentum from IoT and the Edge to HPC

- RISC-V

Why Open Source Hardware?

Software: Leverage a large ecosystem compatible across implementations

Security: A fully auditable collection of IPs: processors, accelerators, etc.

Safety: No black-boxes

SWaP & Customization: SW/HW co-design for exact feature match

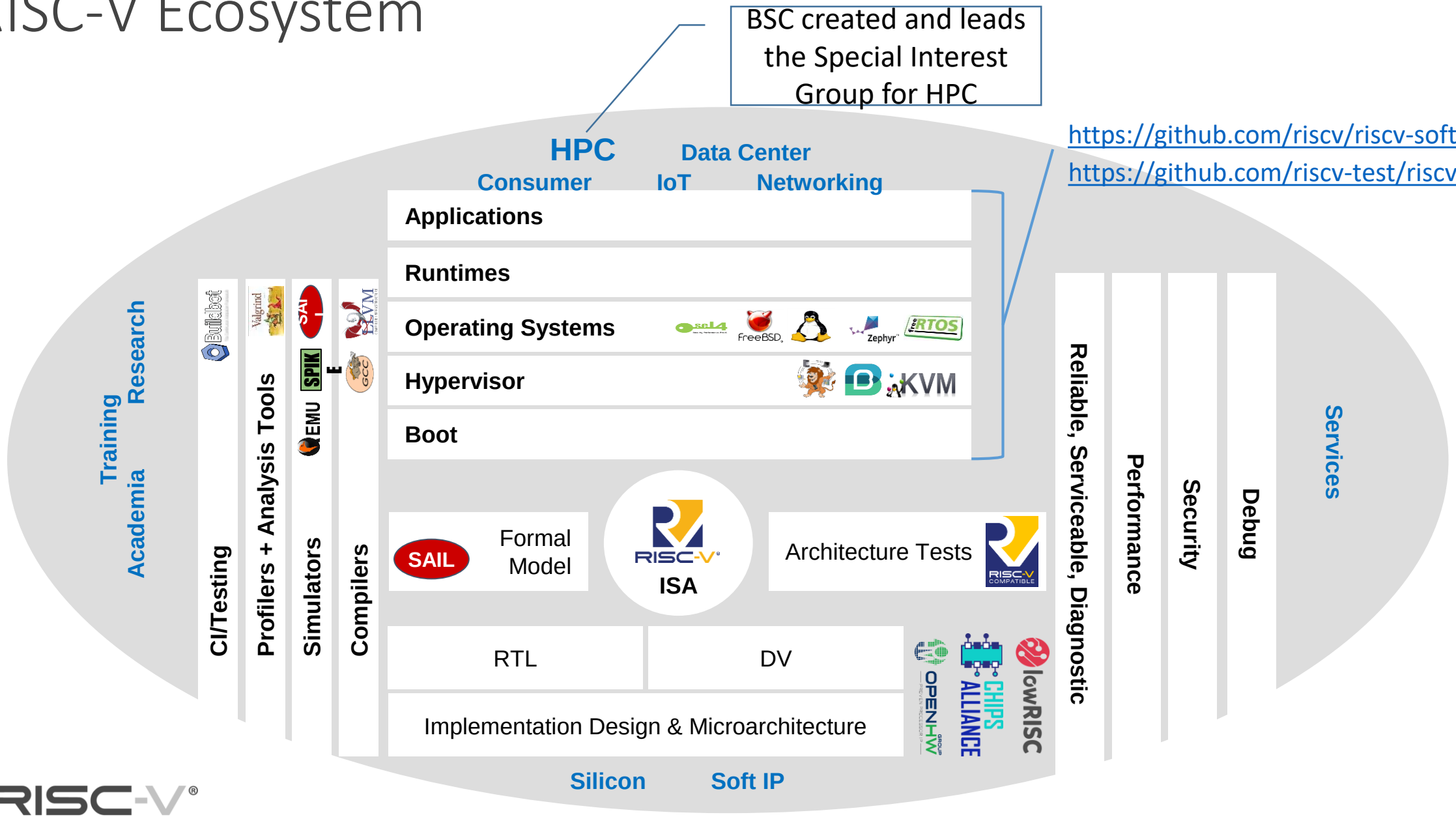
Performance: State-of-the-art implementations

No vendor lock-in: Ecosystem to enable custom develop from SME to large enterprise

Sovereignty: Freedom of access and implementation from design to production

Open Collaboration: Faster time to market, community, leverage existing open source

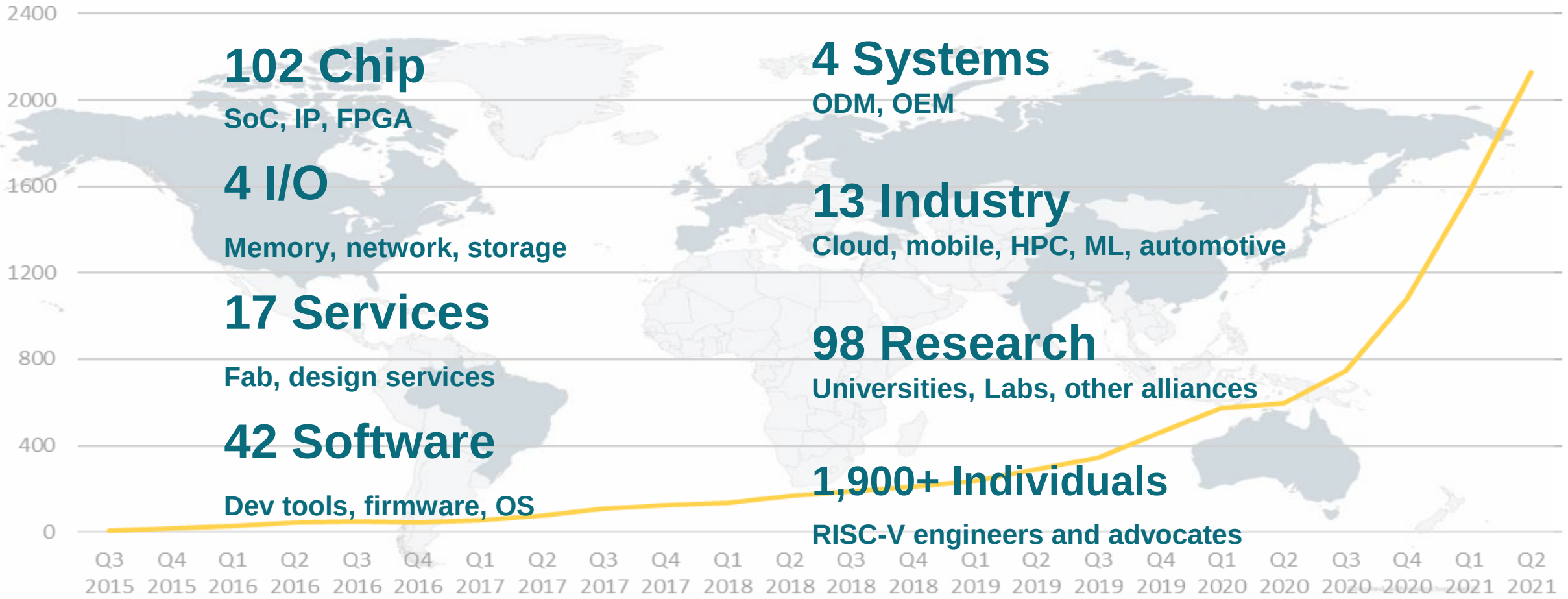
RISC-V Ecosystem



RISC-V®

More than 2,200 RISC-V Members

across 70 Countries



102 Chip

SoC, IP, FPGA

4 I/O

Memory, network, storage

17 Services

Fab, design services

42 Software

Dev tools, firmware, OS

4 Systems

ODM, OEM

13 Industry

Cloud, mobile, HPC, ML, automotive

98 Research

Universities, Labs, other alliances

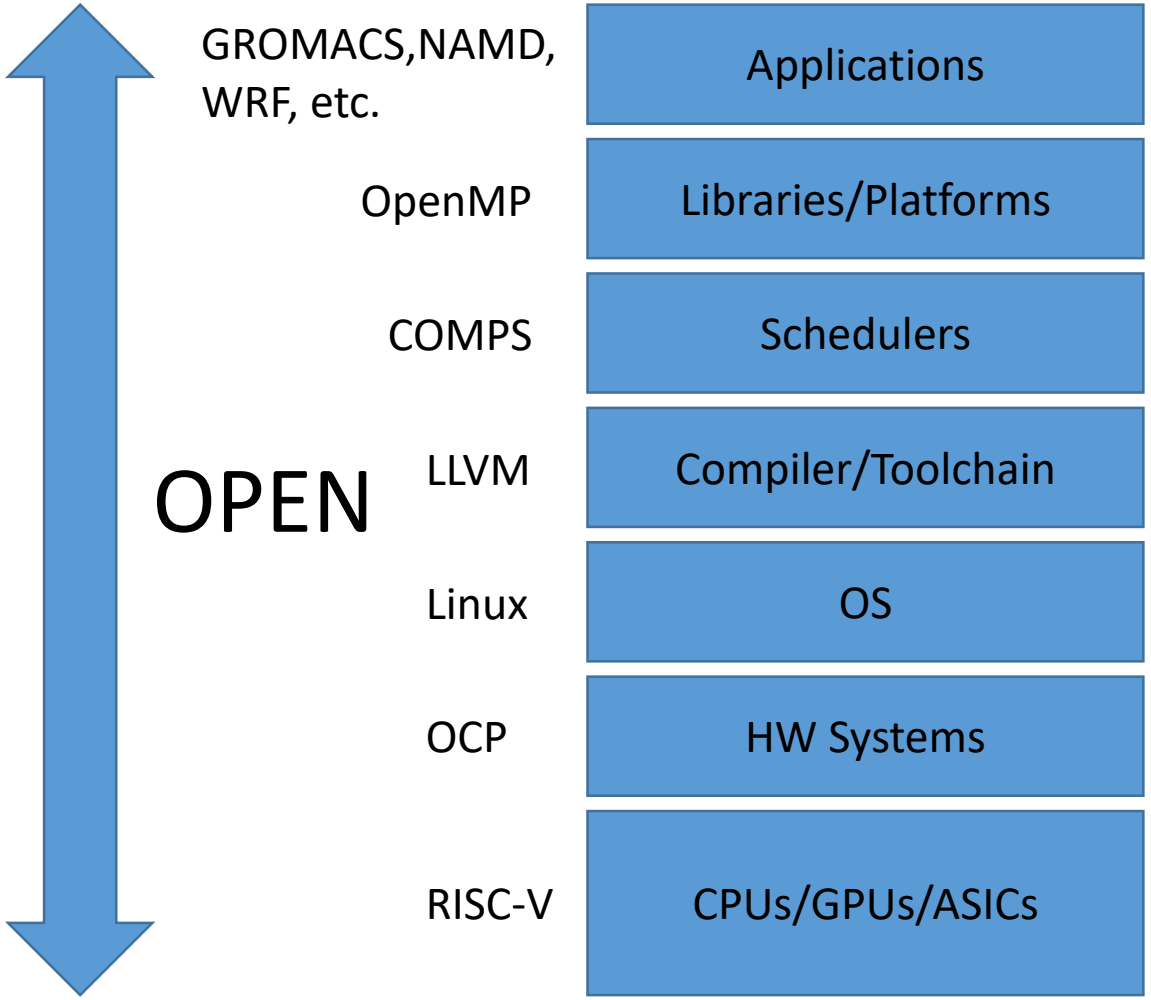
1,900+ Individuals

RISC-V engineers and advocates

RISC-V membership grew 133% in 2020.
In 2021, RISC-V membership has already doubled.

HPC Tomorrow

- Europe can lead the way to a completely **open SW/HW stack for the world**
- RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
- Europe can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- **RISC-V can unify, focus, and build a new microelectronics industry in Europe.**



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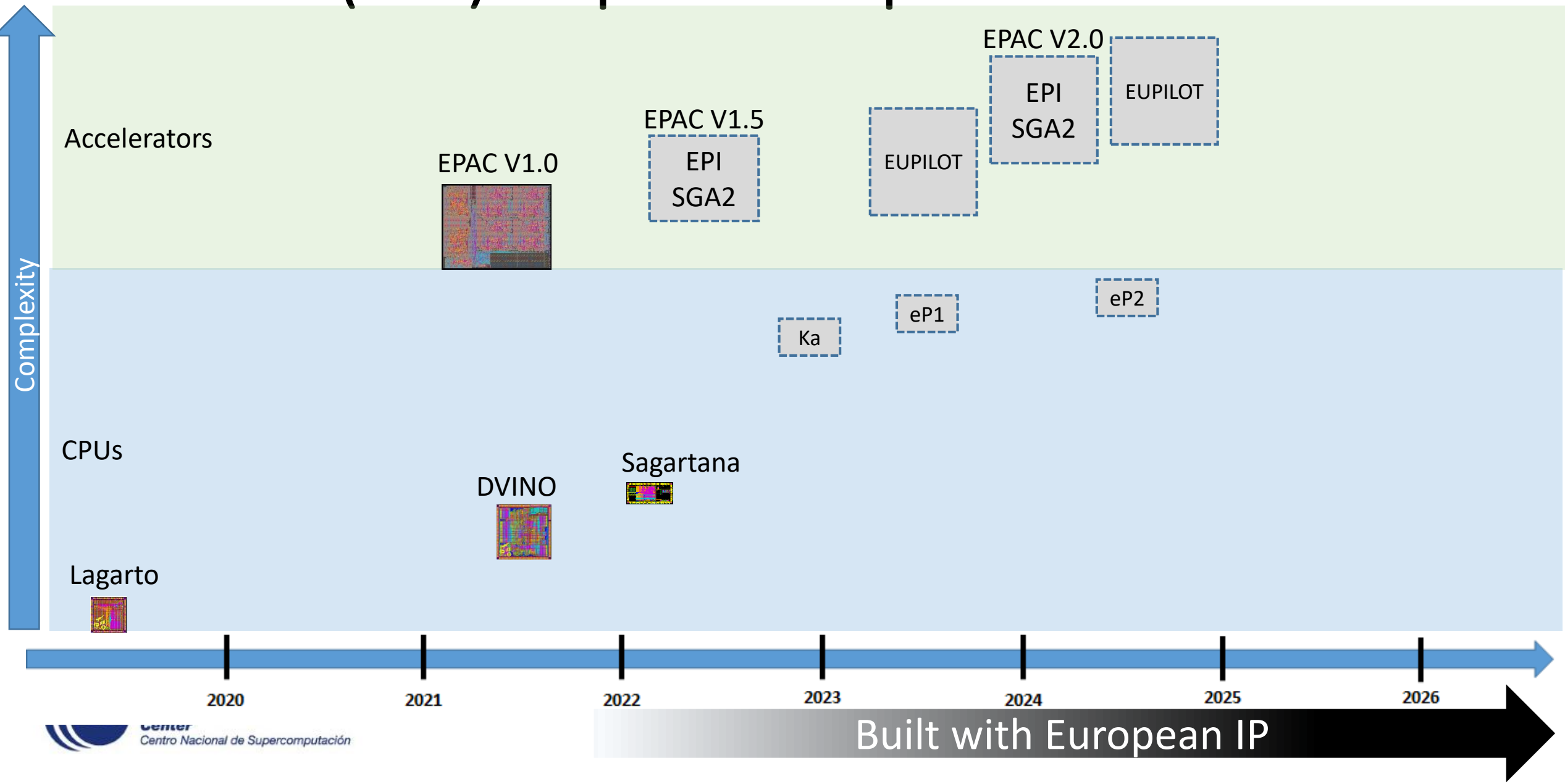
The RISC-V (BSC) Chip Roadmap



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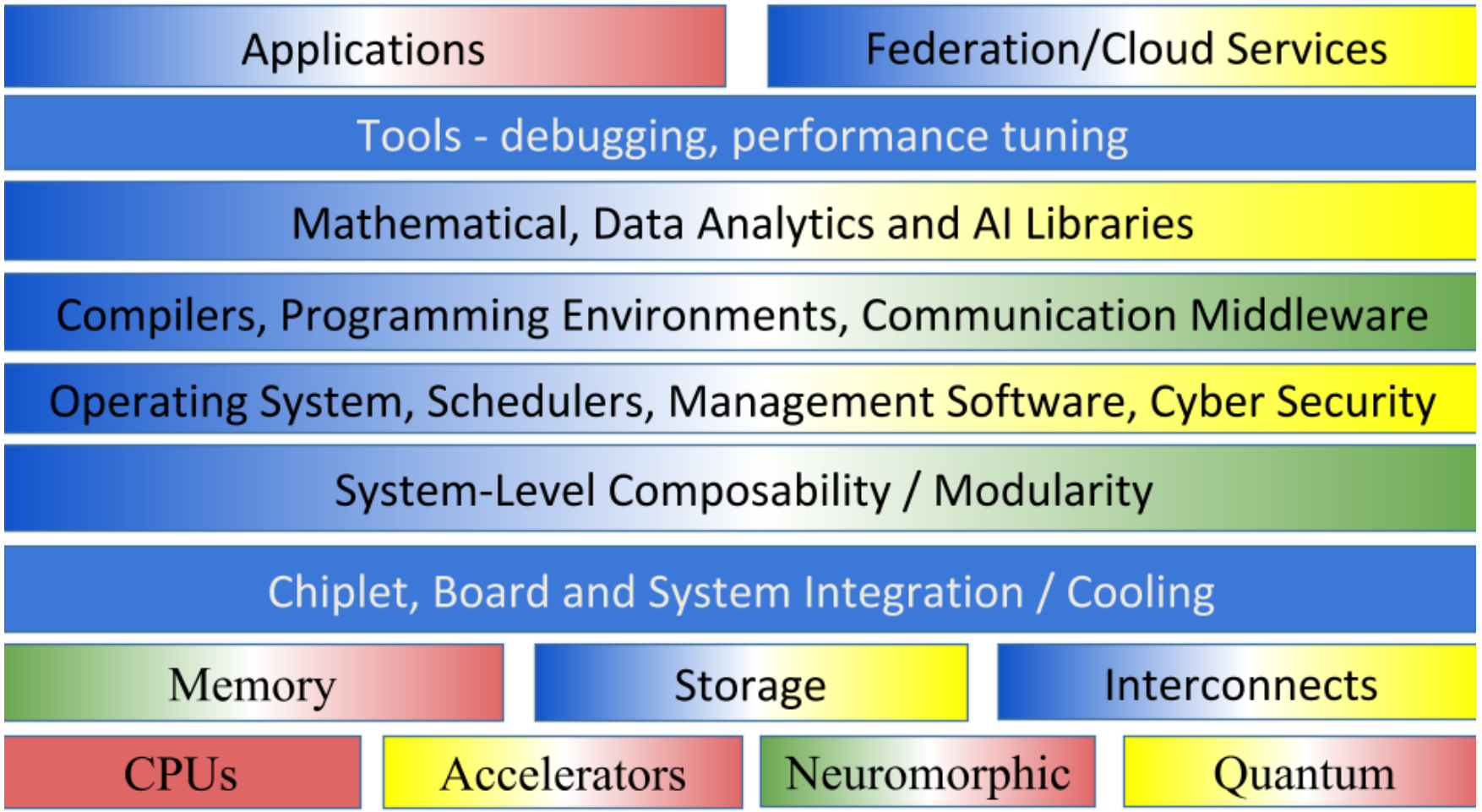
European HPC Stack TRL (from RIAG)



Blue (TRL 8-9) / Green (TRL 5-7) / Yellow (TRL 3-4) / Red (TRL 0-2)

Supporting Open Source

LOCA @ BSC

LOCA

European Laboratory for Open
Computer Architecture

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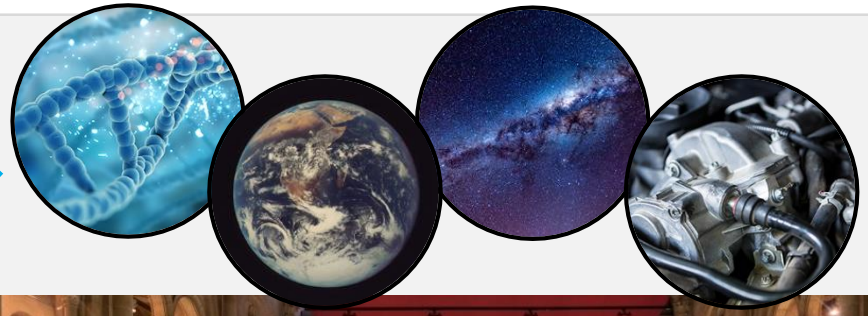
BSC full stack

SW

HW

Software/Hardware Co-Design



HPC Applications

Specialization using HW/SW Co-Design

LOCA
European Laboratory for Open Computer Architecture

HPC Hardware

LOCA

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LOCA Goals

- Mechanism to extend open source ecosystem to include H/W
  - Add H/W expertise to BSC and European partners, leverage existing S/W expertise
  - Provide proven/usable Open Source H/W
  - Intersection of academia and industry
  - Open European IP repository → rapid implementation
  - Catalyst to reinvigorate European ICT industry
  - **Global** collaboration and training center
  - Incubator for European IP

European Collaboration & Education

Casteller

(human tower)

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- Traditional chip design is done in a Master/Apprentice environment
- LOCA recreates this environment by bringing in Masters from industry to collaborate with a variety of people, pushing beyond RTL
- Professors, students, and industry veterans all together
- Ideal sandbox for creative and innovative work
- Research and Design to chip fabrication

SIG-HPC Vision & Mission: RISC-V: IoT to *HPC*

Vision:
The technical and strategic imperatives that guide the RISC-V ecosystem development to enable an Open HPC Ecosystem…

Mission:
…enable RISC-V in a broader set of new software and hardware opportunities in the High Performance Computing space, from the edge to supercomputers, and the software ecosystem required to run legacy and emerging (AI/ML/DL) HPC workloads.

SIG-HPC: An Open era of HPC!

- CPUs, Accelerators, other hardware units, and coprocessors
- Verification and compliance infrastructure and methodologies specific to HPC
- Alignment and engagement and IP enablement.
- RISC-V software ecosystem alignment
- Engage and represent RISC-V in compute intensive industry and academic events
- Identify key industrial and academic partners.
- Support global technology independence with a RISC-V ecosystem roadmap and partners

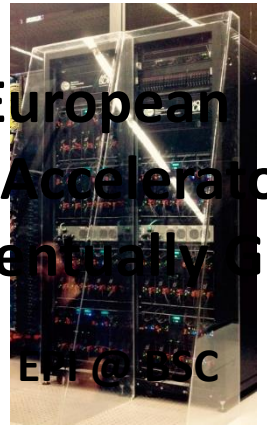
RISC-V®

SIG-HPC Initiatives

- Guide and enable the community
  - Virtual Memory
    - SV57, SV57K, SV64, SV128
  - HPC SW & HW ecosystem & roadmap
  - Accelerators
  - ISA Extensions
  - HPC Software Stack
    - Starting with HPC Libraries

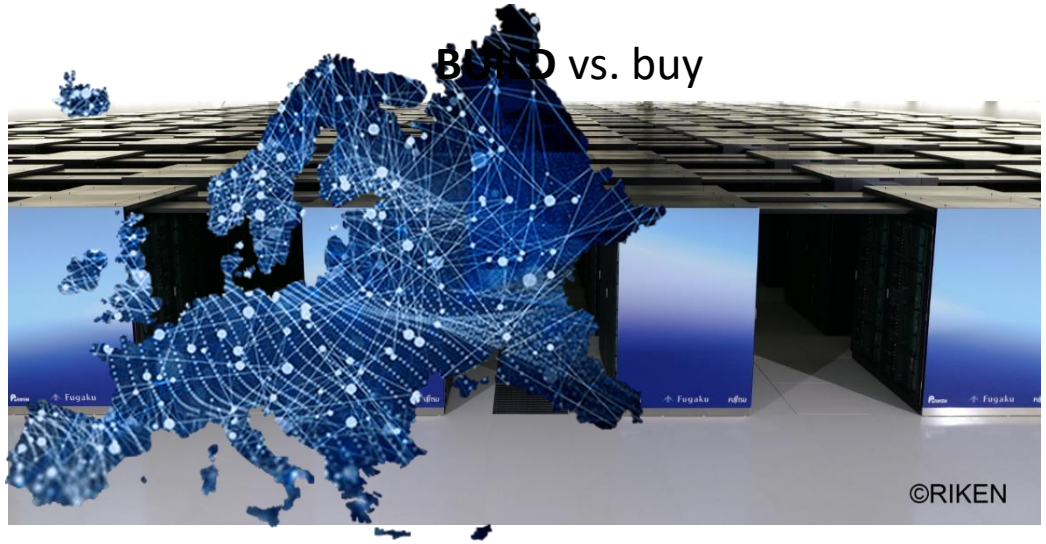
The BSC Vision of the Future of European HPC

European
HPC Accelerators
& Eventually GPP



MontBlanc @ BSC

BUILD vs. buy

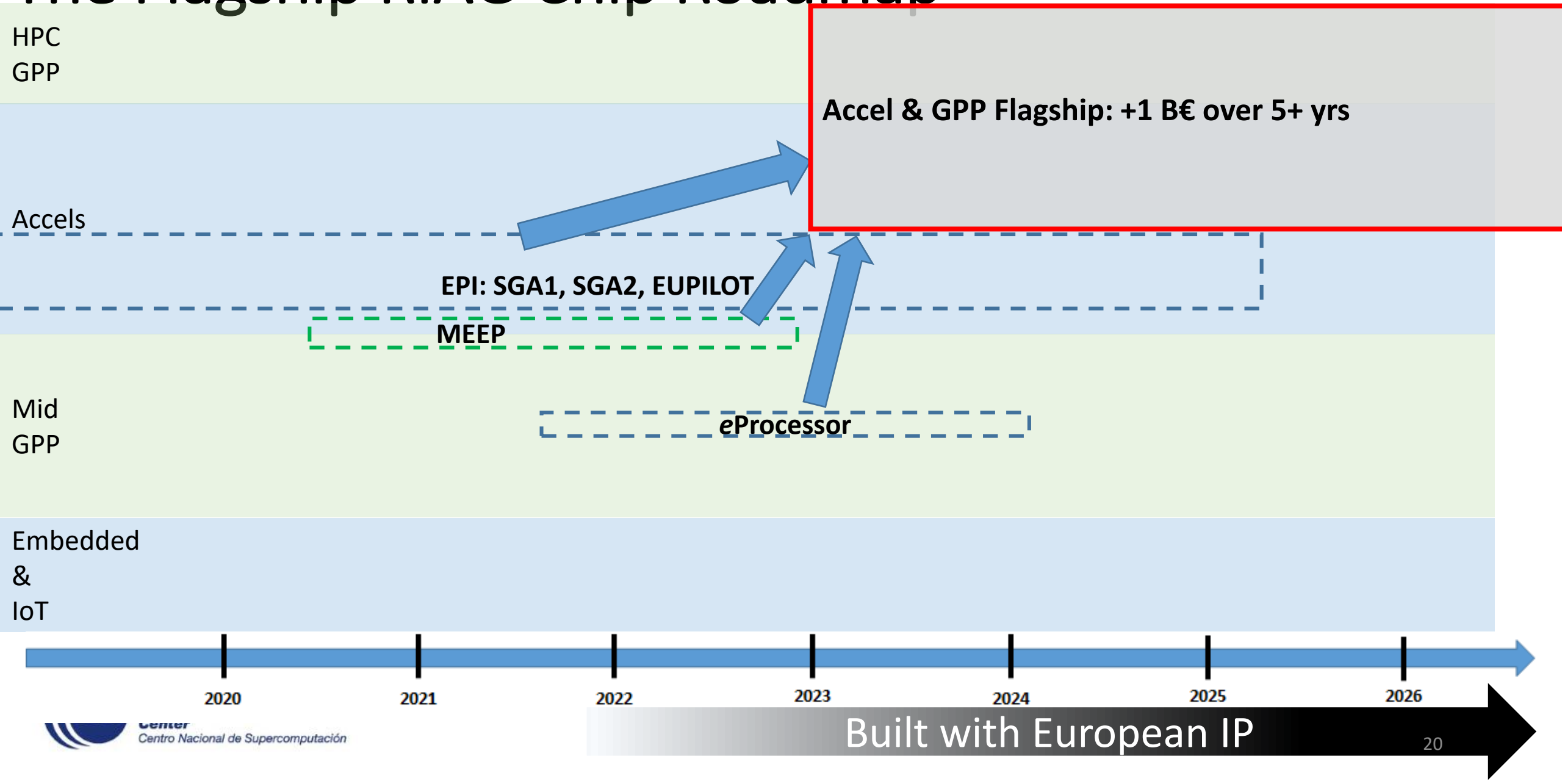


Fugaku #1 Top500 @ Riken for $1B over 7 years (CAPEX)

MareNostrum6

European Supercomputers @ Top500

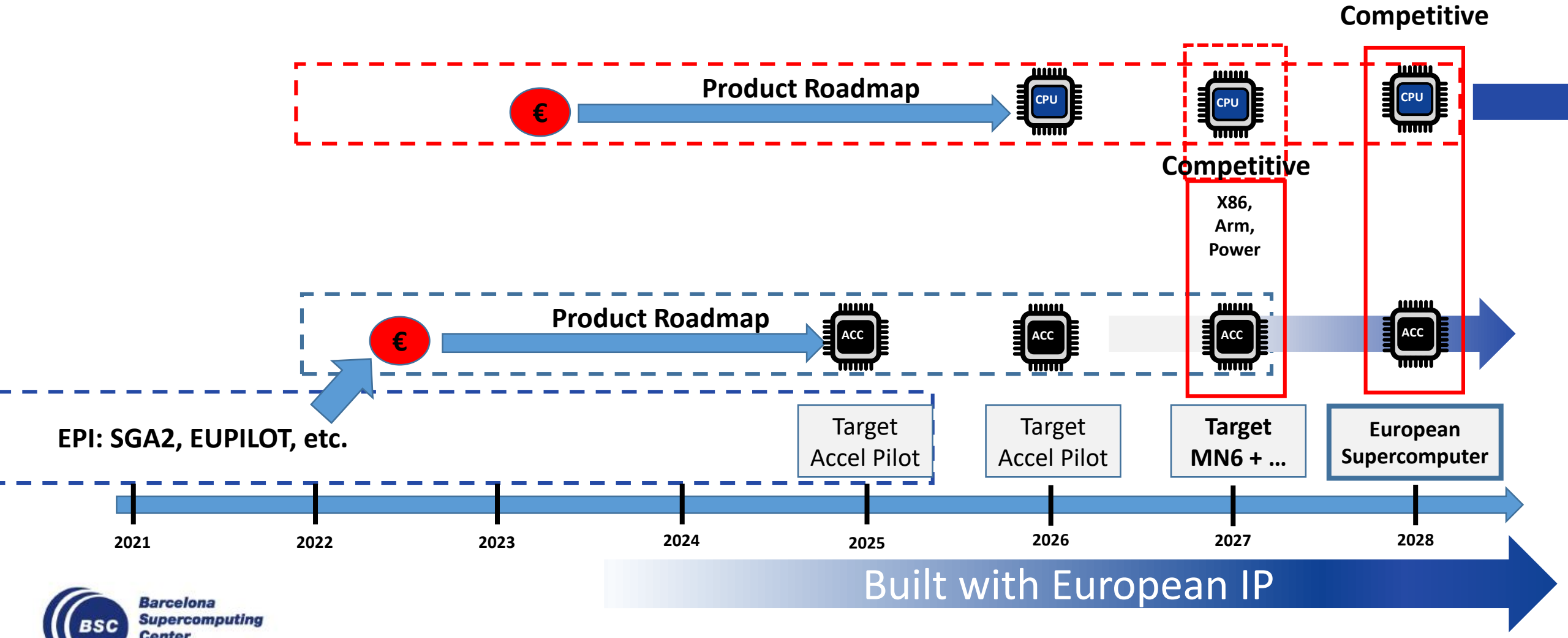
The Flagship RIAG Chip Roadmap



What is the Flagship leading to systems?

- R&**D**
  - Hardware:
    - +1 B€ & Small number of partners
  - Software
    - +1 B€ Leverage EU ecosystem and many partners
- System Integrator
- RISC-V HPC Accelerator, then GPP
- Precursor to the Machine tender
- Examples
  - Fugaku: +$1 B **D** + $1 B system (over 6+ years)
  - ECP: $2 B (HW+SW) **D** + $1.8 B for 3 systems

Ideal RISC-V Timeline for a European Supercomputer



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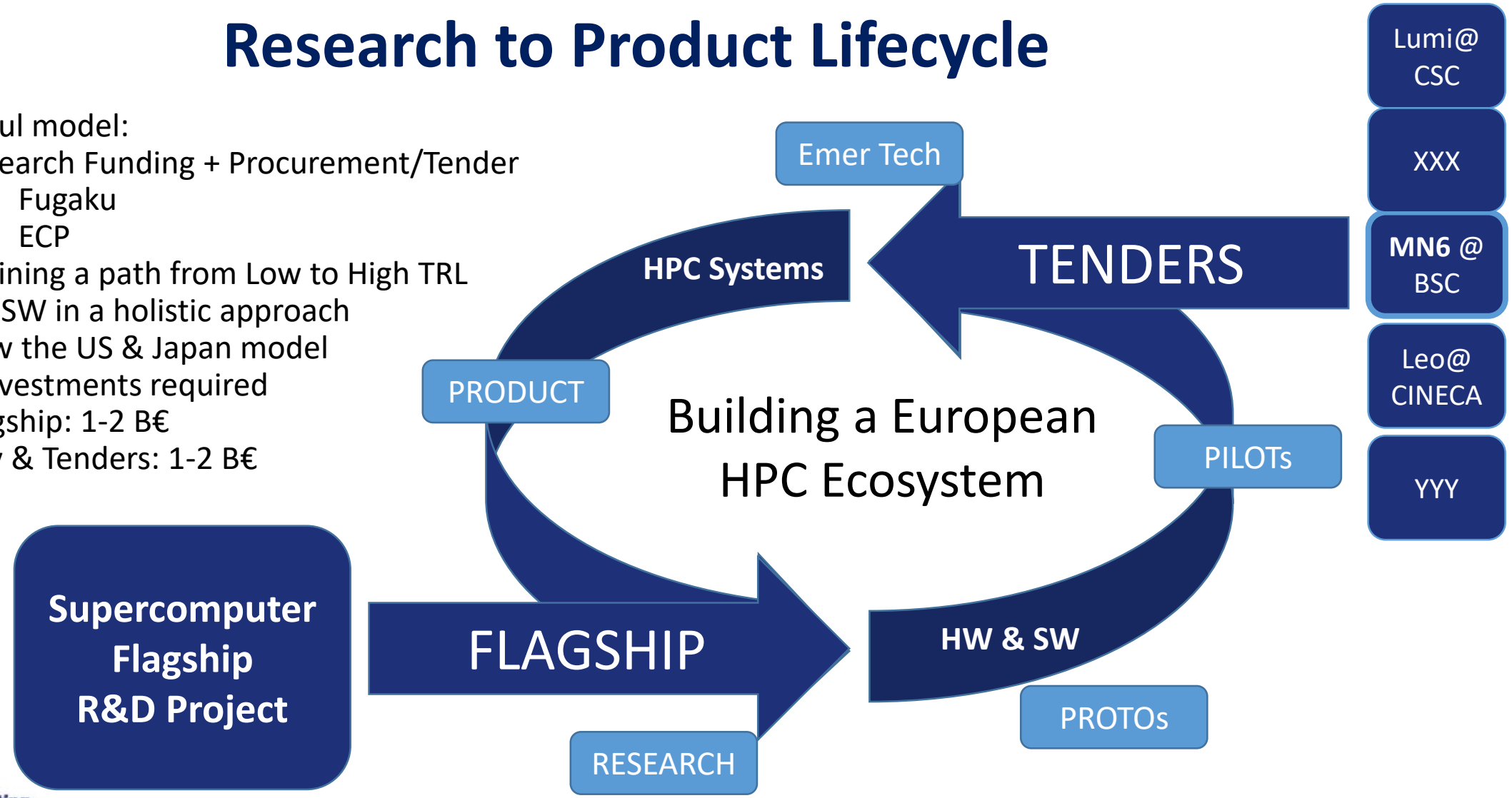
Research to Product Lifecycle

- Successful model:
  - Research Funding + Procurement/Tender
    - Fugaku
    - ECP
  - Defining a path from Low to High TRL
- HW and SW in a holistic approach
- EU follow the US & Japan model
- Major investments required
  - Flagship: 1-2 B€
  - Dev & Tenders: 1-2 B€



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A Successful EC Roadmap for the Future

- Embrace Open Source Hardware
  - Build infrastructure to support open source
  - Create an environment that links research to the ICT industry
  - Supported by research and industrial funding instruments
- Teach, train, tools, and collaborate (Skills)
- Center of Excellence for Open Systems
  - EuroHPC to KDT and Chip
  - Multiple streams aligned to domains
- Leverage the Global Technology ecosystem (Systems)
- “Made in Europe” HPC requires **SIGNIFICANT** funding for programs
  - Many **focused** projects
  - Many **focused** teams
  - Total and integrated vision for the future: Build vs Buy…
  - Large Accelerator and CPU investment SW and HW **(> 1B€, each**)

Discussion

- Can we use the MN6 as a pilot development for HPC systems to support Build & Buy?
- What is European?
- Where do we find the (European) money to kickstart the value chain?
- Which applications or domains?
- How do we cross the TRL chasm?
  - Funding, ownership, …
- What is missing in the ecosystem today? Not addressed by commodity solutions…
  - Is there any differentiation?
- Unified plan to support European HPC?
- Other parts of the system: interconnect, storage, power delivery,…
- New technologies:
  - Quantum
  - Neuromorphic
  - Etc.
- Cloud technologies?
- Insert your questions and comments here …
- 3B4HPC 2: June 29-30, 2023?

Thank you

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