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SiPearl in EPI
3B4HPC, July 1st, 2022

Jean-Marc Denis
Chief Strategy Officer
jean-marc.denis@sipearl.com

Company Update

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SiPearl corporate overview

The European Server Processor Solution

HQ: Maisons-Laffitte (Paris), France

Incorporated in June 2019

CEO and Founder, Philippe Notton

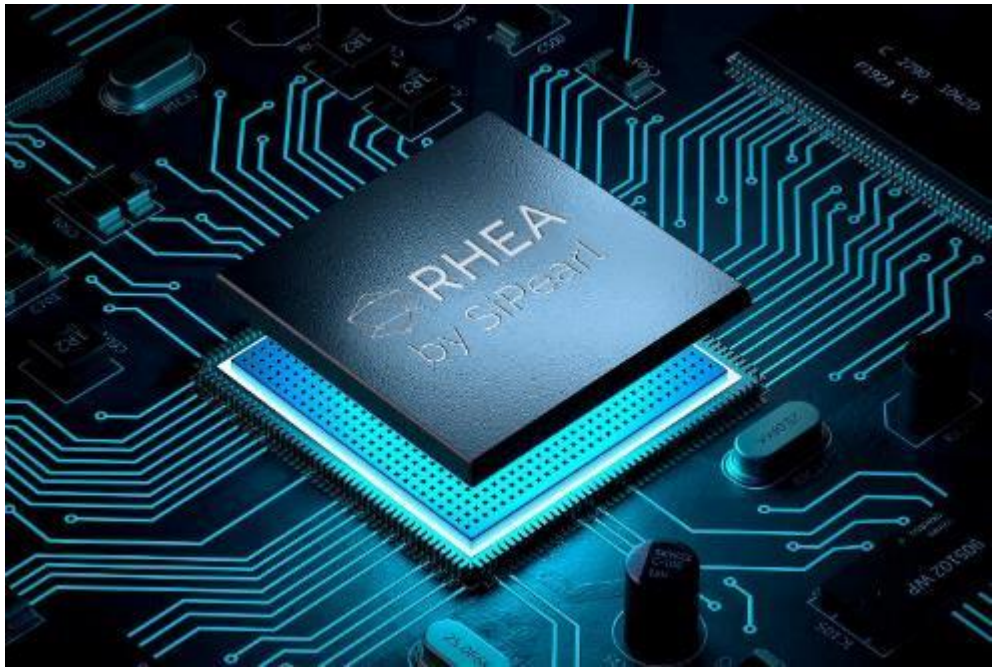
Design centers:

- France: Maisons-Laffitte, Massy, Sophia Antipolis, Grenoble
- Germany: Duisburg (Düsseldorf)
- Spain: Barcelona

Key Personnel from Intel, Atos, ST, Marvell, Nokia, Mstar-Mediatek

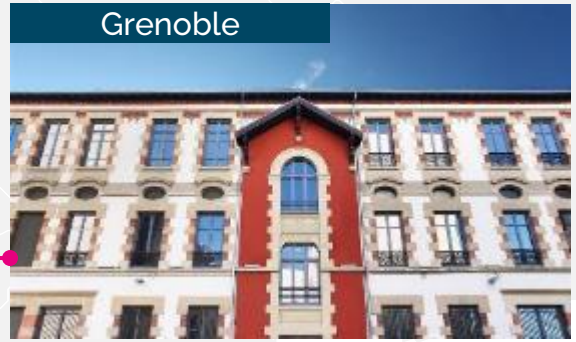
HPC Targeted Architecture based on Arm Neoverse V1 cores

109 employees today, targeting >1,000 in 2025



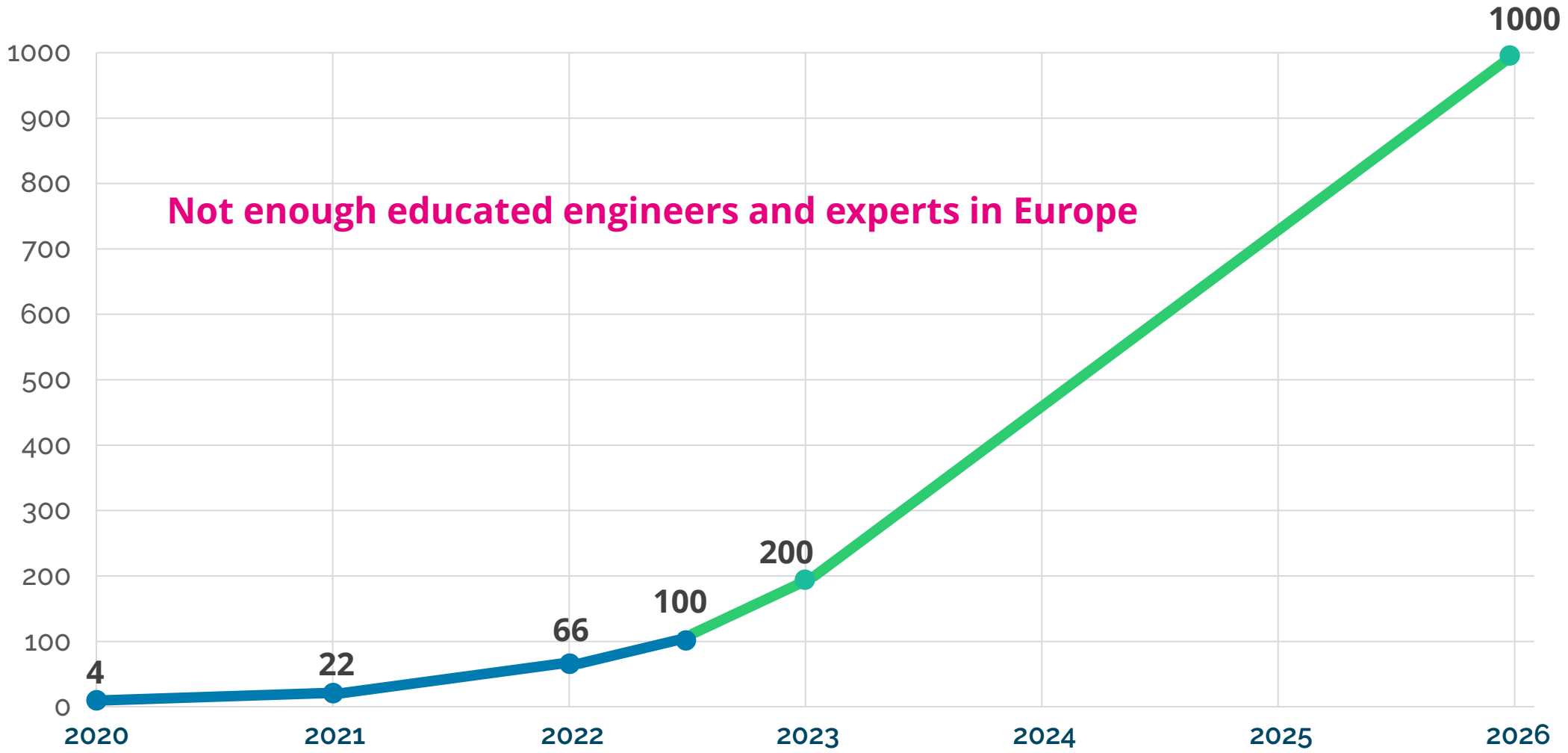
SiPearl offices

We are close to our partners and customers



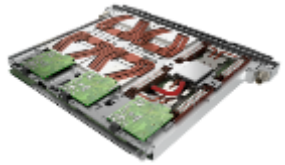
Official requests for new offices from local Trade Agencies: Italy, Switzerland, Canada

Headcount evolution 2020-2025



Partnerships and ecosystem

Atos



Atos HPC Software Suites

RISC-V

oneAPI

LLVM COMPILER INFRASTRUCTURE

open source

NVIDIA CUDA

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Hewlett Packard Enterprise

HPE Cray Programming Environment

epi European Processor Initiative

GRAPHCORE

intel

NVIDIA

More Coming Soon!

arm

European Processor Initiative

epi

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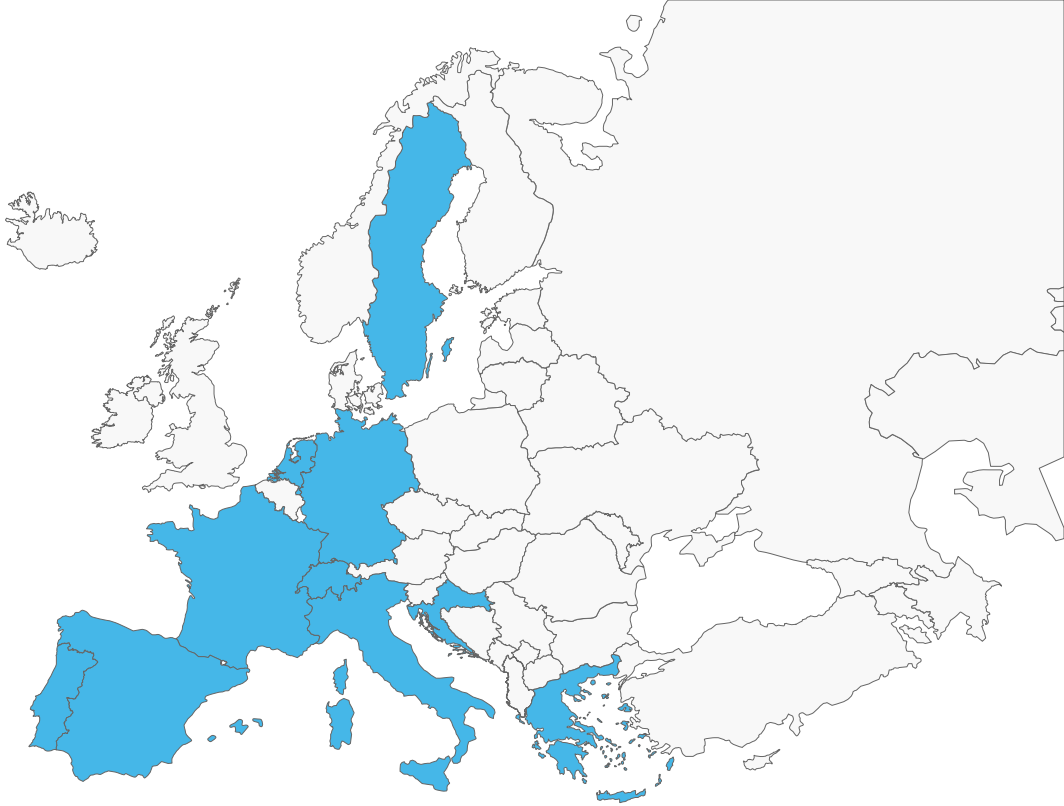
EPI project factsheet

Phase 1 successfully concluded (2019-2021)

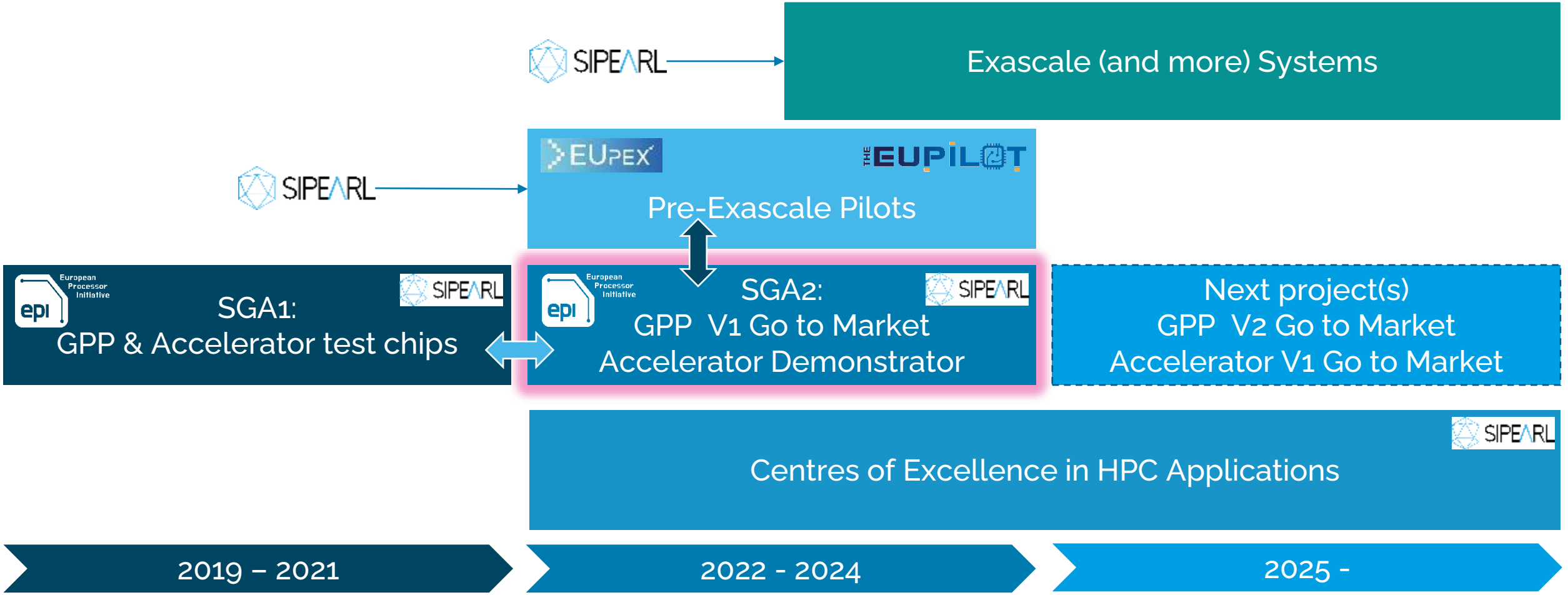
Currently in Phase 2 (2022-2024)

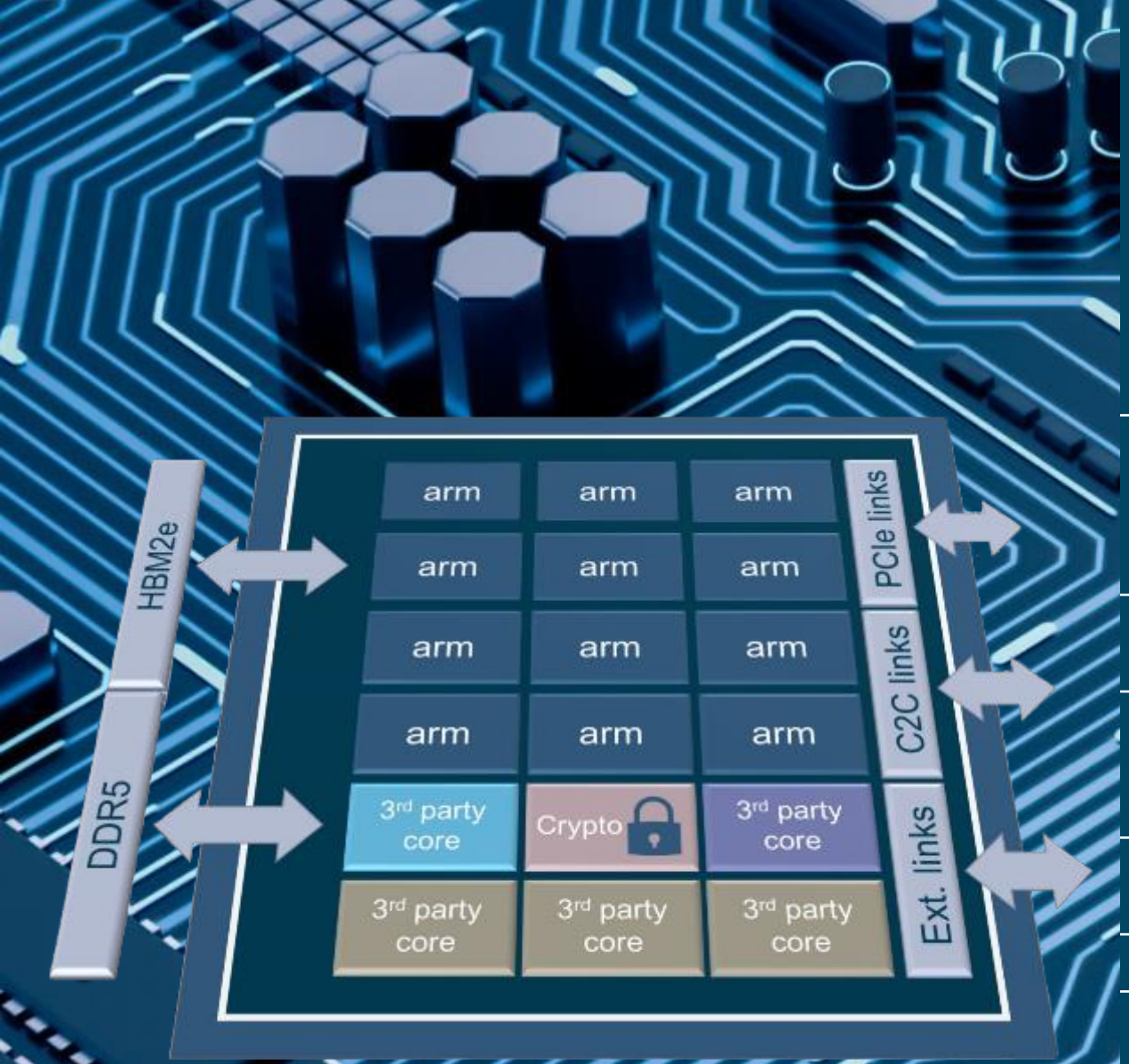
Consortium of 30 European academic and industrial partners from 11 countries

Funded by EuroHPC JU (50%) and co-funded by Croatia, France, Germany, Greece, Italy, the Netherlands, Portugal, Spain, Sweden and Switzerland



The ecosystem road to EU Exascale

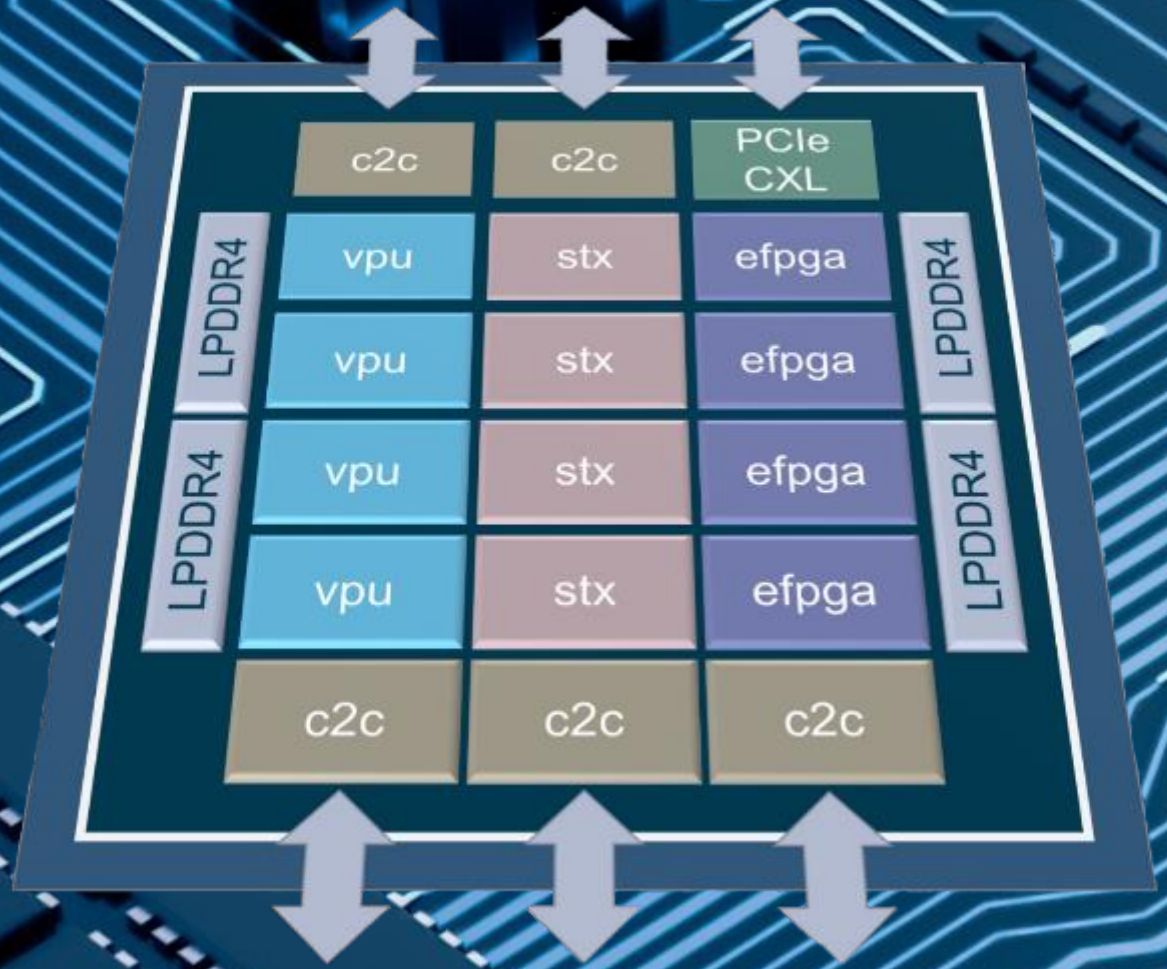




Rhea

General Purpose Processor family

Core	- Arm architecture - Neoverse V1 cores - SVE 256 per core supporting 64/32/BF16 and Int8 - ArmVirtualization extensions
SoC	- Arm mesh fabric - Advanced RAS support including Arm RAS extensions - Link protection for NoC & high-speed IO - ECC support for selected memory
Cache	- Large L3 (Shared Level Cache) - RAS supported for all cache levels
Memory	- HBM2e - And DDR5 - ECC for memory and link protection for controllers
High Speed I/O	- PCIe, CCIX & CXL - Root and endpoint support
Other I/O	- USB, GPIO, SPI, I^2C
Power Management	- Power management block to optimize perf/watt across use cases and workloads.
Security Block Support	- Secure boot and secure upgrade - Crypto - True random number generation - Made in Europe



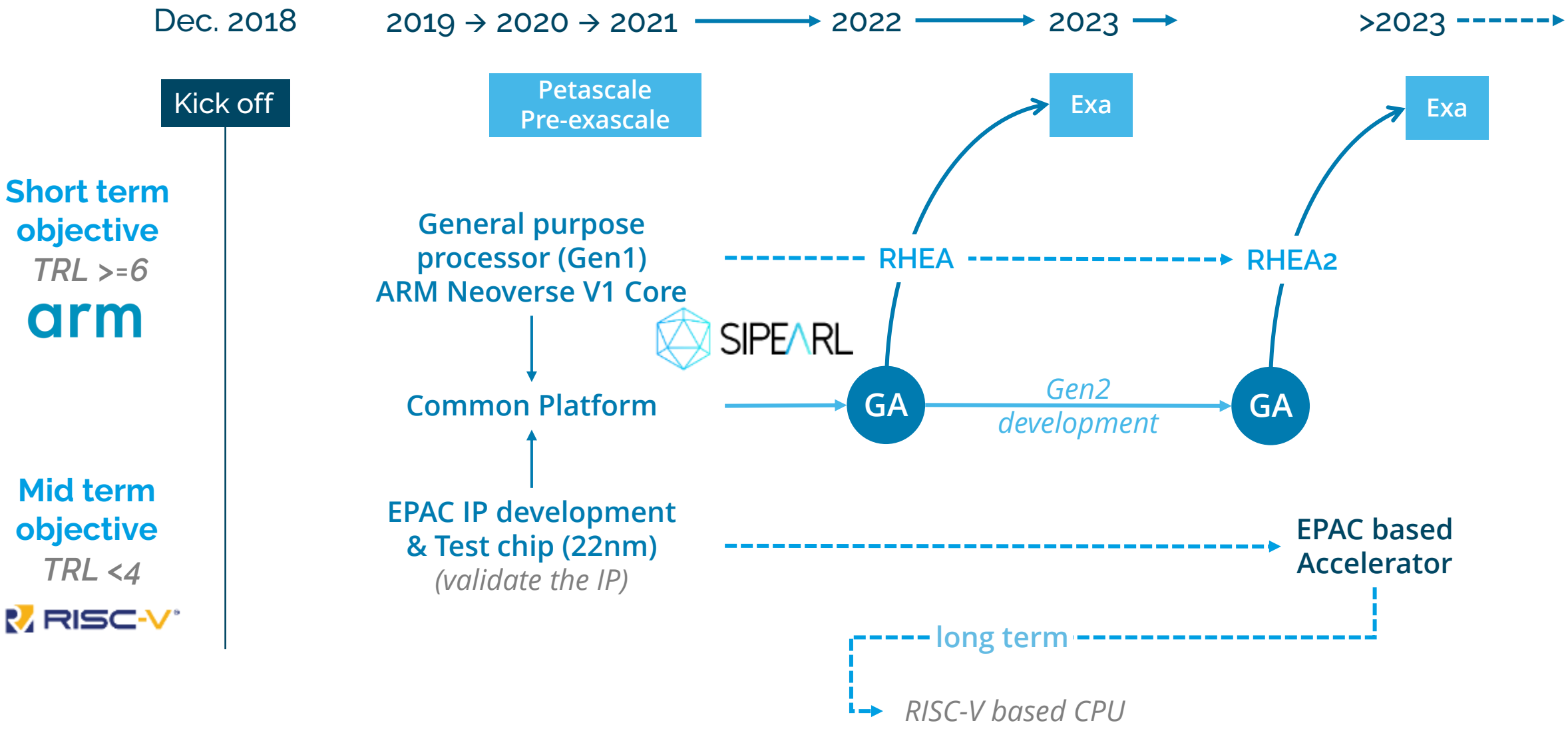
EPAC

Accelerator Processor family
Risc-V ISA based

- vpu – Vector Processing Unit
- stx – Stencil/Tensor accelerator

- The first generation of commercial EPI GPP validated
- Integrated into EU state of the art data centers

Overall roadmap: combine build and buy



EPI Common Platform enables EU Ecosystem

SiPearl chartered is also to develop the European Ecosystem

SiPearl shares IP and benefits from IP ecosystem

Accelerator development (RISC-V based)

- AI (tensor)
- Vector processing
- Stencil processing
- FPGA

…

Packaging

IP development

Staged integration: start with socket-to-socket connections and move into package (multi-chiplets) over time

Now: buy IP

Future: build IP (10y?)

The road to sovereignty

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Sovereignty is coming on the top of classical business sustainability

HPC Supercomputing

SiPearl entry business: European HPC

2023

HPC-dedicated

Data Center-Central

Data centers, private and public cloud

2025

DATA CENTER

Public cloud

Private cloud

Embedded Security channel

Data Center-Edge

Smaller Data centers,
including around 6G infrastructure

2027+

6G infrastructure

Our business model is sustainable over time

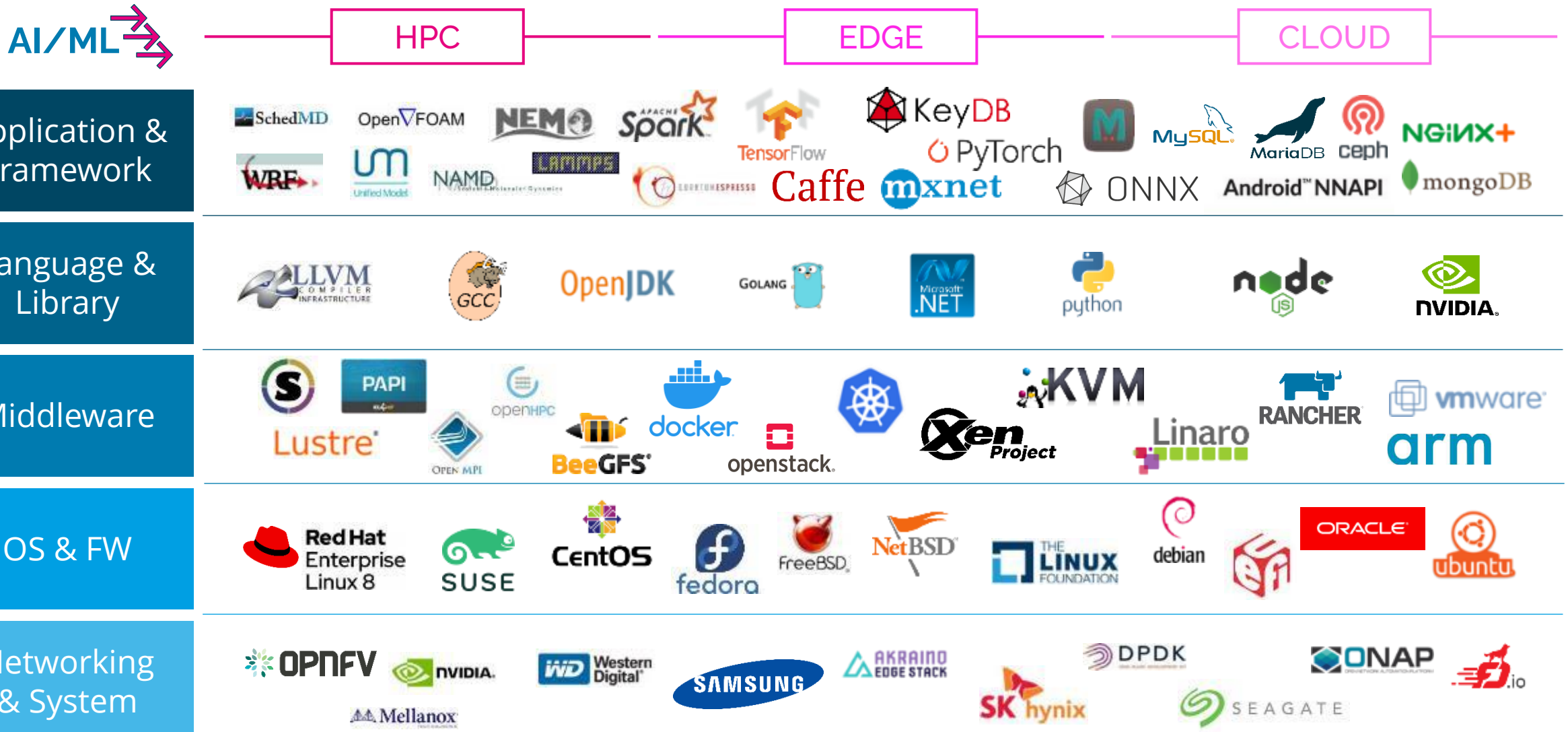
Rhea: Designed in Europe

Total: x V1 + 2 M7 Arm, 29 Risc-V, 4x SPUs.			Remarks
Arm Neoverse V1 cores	Arm Neoverse V1	arm	Including spare V1s.
Arm cortex-M7 cores	2x Arm cortex-M7 = 2.	arm	for SCP and MCP subsystems.
Risc-V in PMS	1x Ariane + 1x ZeroRiscy = 2.	RISC-V	
Risc-V in SEG	1x Ariane = 1.	RISC-V	SEG for security element.
Risc-V in STXs of 2x ERACs	2x (1x Ariane + 8x Snitch) = 18.	RISC-V	Snitch is a EU IP (stencil + tensor)
Risc-V in VRPs of 2x ERACs	2x (4x VRP core) = 8.	RISC-V	VRP core is a modified Risc-V core.
SPUs in STXs of 2x ERACs	2x (2x SPU cores) = 4.	RISC-V	SPU core is a EU IP.

- Some additional EU designed IP (power management, clock, cryptography) not counted here
- Not including µC cores used in Synopsys DDR controllers for the PHY training.
- ERAC: tests features, perf/mm2 and perf/w in 6nm. Competitiveness?

Core	Performance for the core.
V1	2x 256 SVE = 16 DP FLOPs/cycle; 2.5GHz@N6
Snitch	1x 64b FPU = 2 DP FLOPs/cycle; >1GHz@N6
SPU	4x 32b FPU = 8 SP FLOPs/cycle; >1GHz@N6

Arm Software Ecosystem: the most exhaustive, Open and proprietary
Is Sovereignty a concern?



Software stack: EU is already 100% sovereign. HPC centers & EuroHPC play a central role.

We rely on standards to ensure portability and compatibility for the customers; and to avoid vendor lock-in. Our goal is to make our design easy to use efficiently, including in the software stack by avoiding proprietary elements wherever feasible.

ISA:

Short-Mid term: ARM

Long term: RISC-V or ARM

- Gated by ecosystem, liability, fragmentation, …

Preferred SW partners:

OpenSource communities

ARM

System OEMs

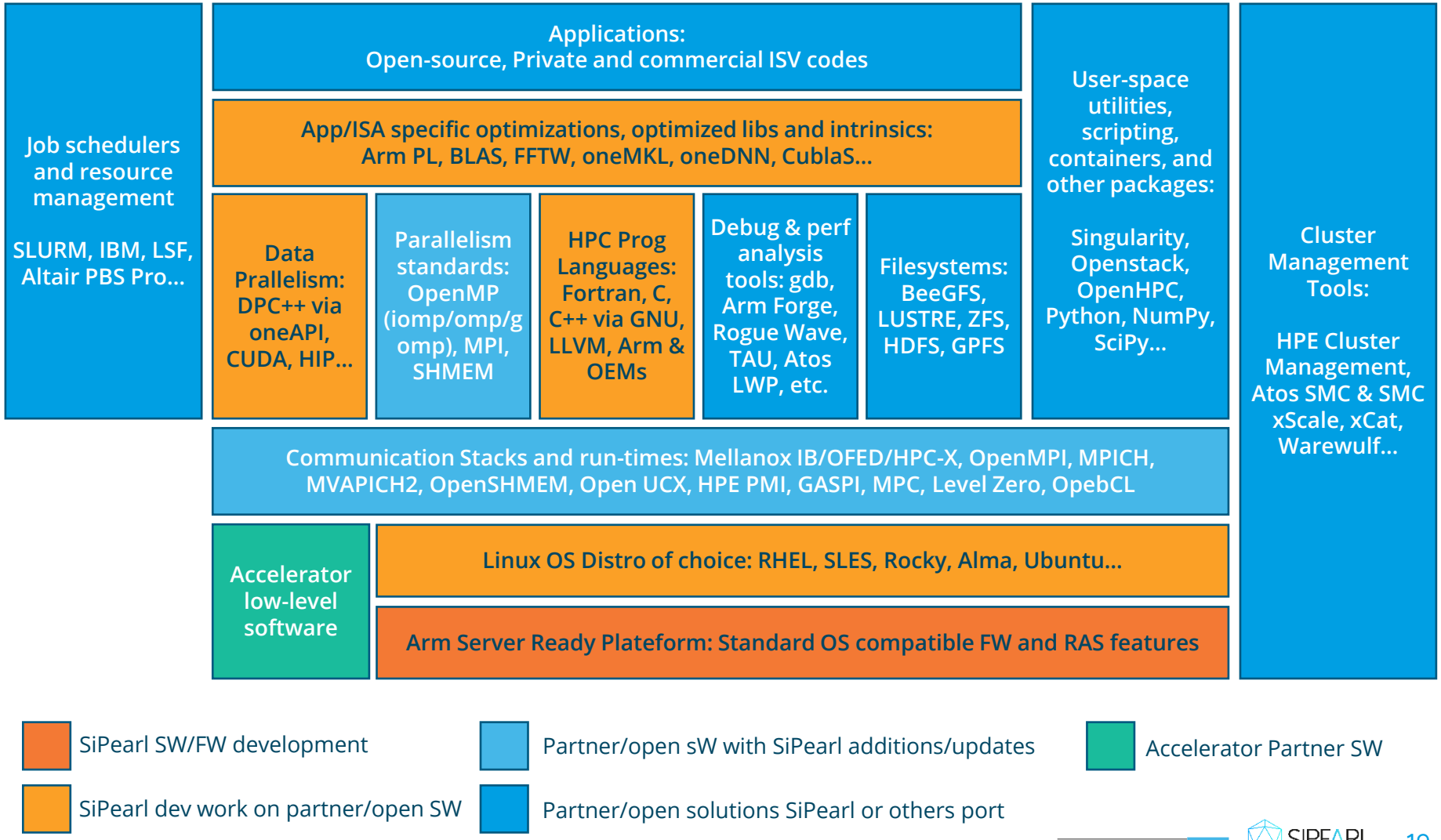
Accelerator partners

- Graphcore
- Intel (oneAPI/SYCL…)
- Nvidia
- …

ISV and System stack providers

Cloud solution ecosystem

- Azure
- AWS
- …



Build and Buy

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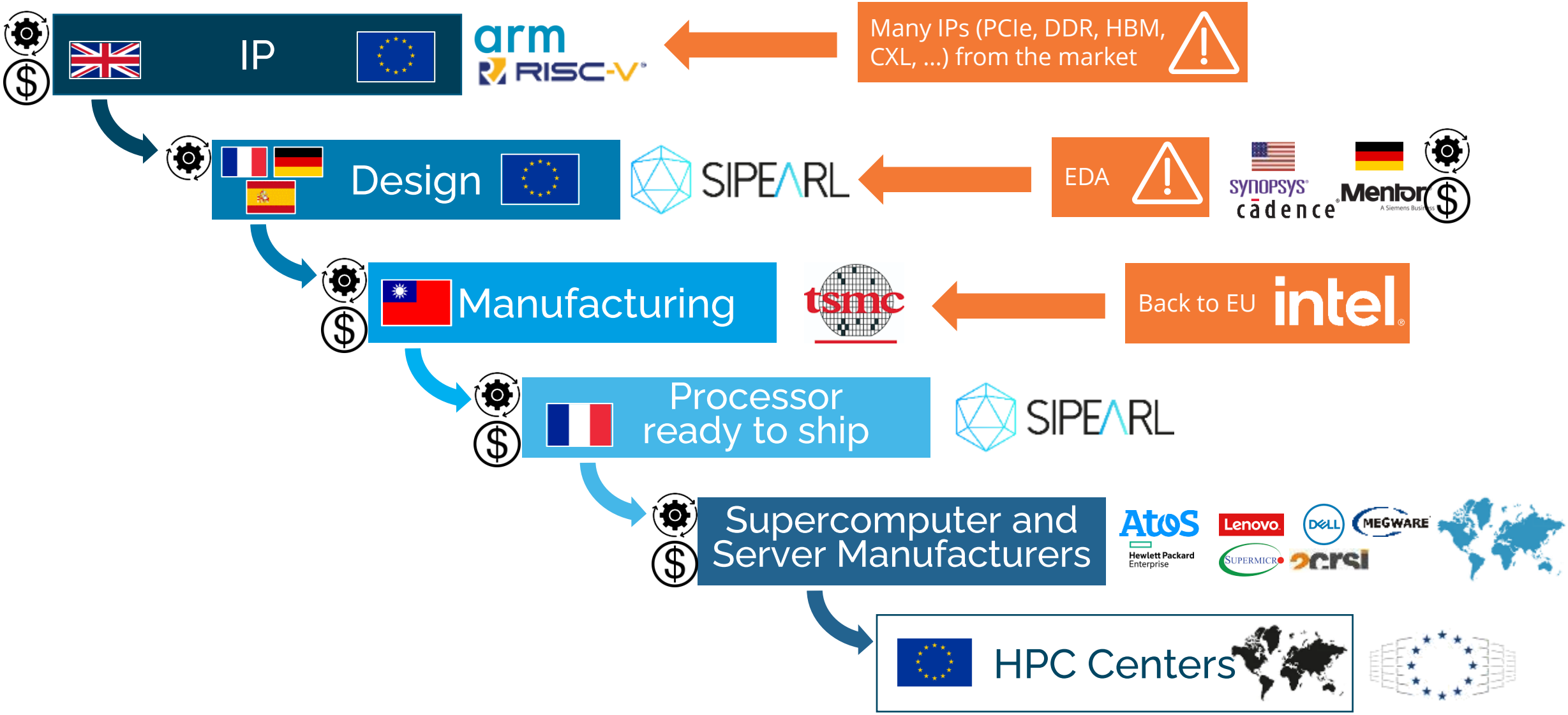
Build vs buy $: Value chain




The
Elephant
in the Room


VENTURE
CAPITAL
INVESTMENT
COMPANIES
BUSINESS
HIGH
FIRM
PRIVATE
CAPITALISTS
FUNDING
GROWTH
TECHNOLOGY
INVESTMENTS
RETURN
POSITIONS
DEBT
DEALS
LOAN
VC
LIMITED
BANKING
INVESTING
INTEREST
POOL
REFERRED
NOVEL
SENIOR
PRINCIPAL
TEND
REALIZING
INDUSTRIES
MAKES
ONE
POTENTIALLY
DIFFERENT
ADDITION
BIOTECHNOLOGY
POTENTIAL
INVESTS
POSITION
INVESTORS
WITHIN
COMPANY
SIGNIFICANT
LARGE
CASE
NETWORKS
VALUE
TYPICAL
ALTHOUGH
CONSULTING
FUND
BACKGROUNDS
MANAGEMENT
SOURCE
ASSOCIATE
ANOTHER
USUALLY
FIELD
EQUITY
FUNDS
ROUND
RETURNS
FIRMS
NEW
STARTUP
OPERATIONAL
KNOWN
FINANCE
STAGE
RISK
MANAGING
MANY
OFTEN
PUBLIC
MONEY
PARTICULAR
EXPECTED
FINANCIAL
FORMAT
MOVE
THEREBY
TYPICALLY
PARTNERS
EXPERIENCE
OPERATING
RATES
YEARS

About SiPearl

Created by Philippe Notton, SiPearl is designing the high-performance, low-power microprocessor for European exascale supercomputers. This new generation of microprocessors will enable Europe to set out its technological sovereignty in strategic high performance computing markets such as artificial intelligence, medical research or climate modelling.

SiPearl is working in close collaboration with its 27 partners from the European Processor Initiative (EPI) consortium - leading names from the scientific community, supercomputing centres and industry - which are its stakeholders, future clients and end-users.

SiPearl employs 110* people in France (Maisons-Laffitte, Grenoble, Massy, Sophia Antipolis), Germany (Duisburg) and Spain (Barcelona).

The company is supported by the European Union (funding from the European Union's Horizon 2020 research and innovation program under specific grant agreement no.826647).

* as of June 30th 2022

Contact
Jean-Marc Denis
Chief Strategy Officer
jean-marc.denis@sipearl.com